

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DATE	AN	

Filed: New Application "SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURING METHOD"
Attorney Docket: 32011-168503
1 of 19
Inventor: Toyokazu SAKATA et al.

FIG. 1(A)

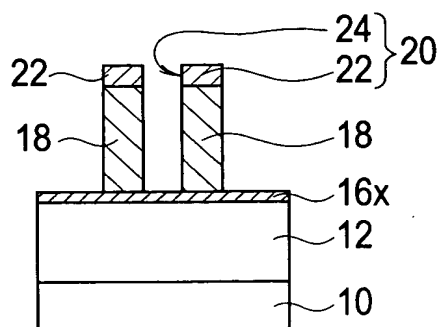


FIG. 1(B)

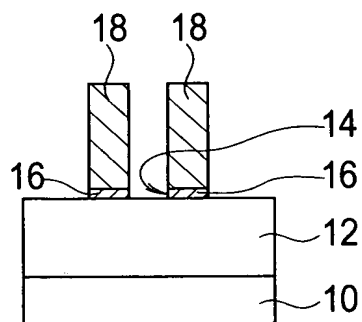


FIG. 1(C)

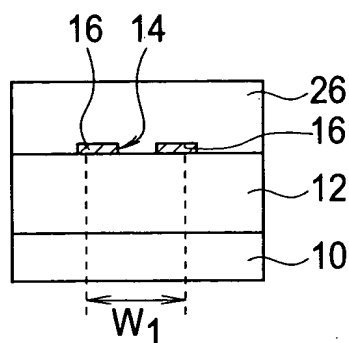


FIG.2(A)

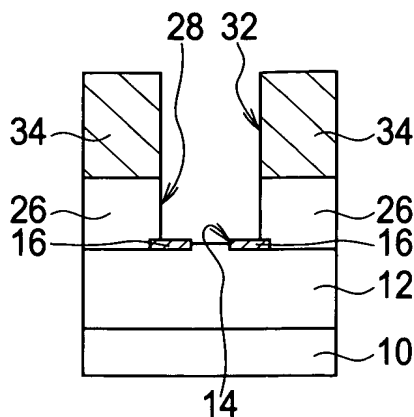


FIG.2(B)

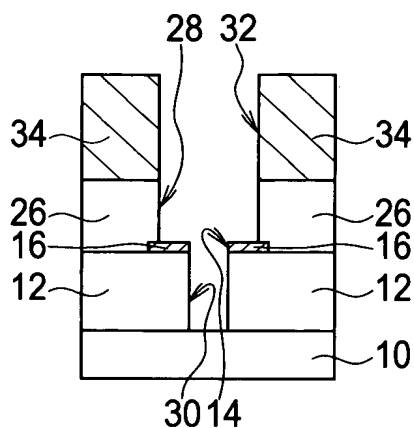
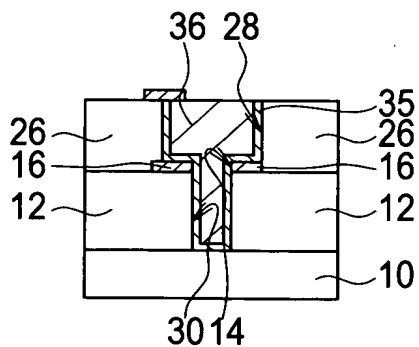


FIG.2(C)



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FIG. 4(A)

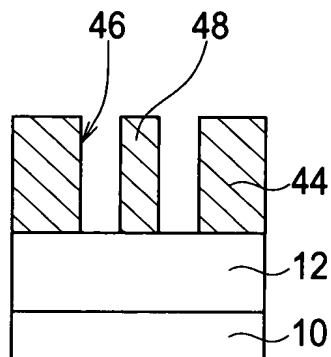


FIG. 4(B)

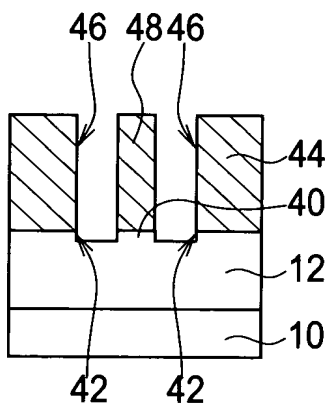


FIG. 4(C)

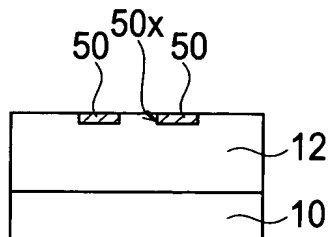


FIG. 5(A)

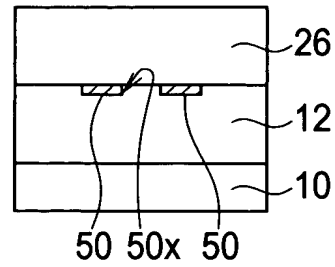


FIG. 5(B)

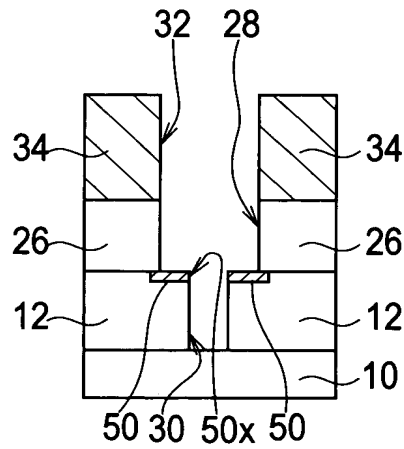
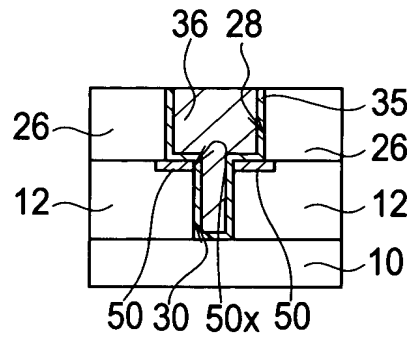


FIG. 5(C)



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FIG. 6(A)

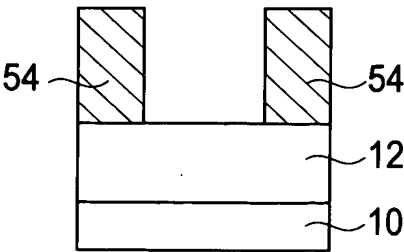


FIG. 6(B)

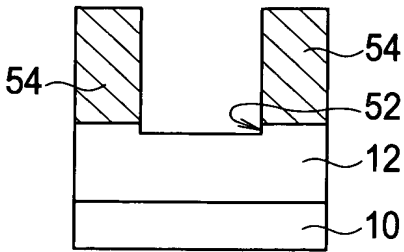


FIG. 6(C)

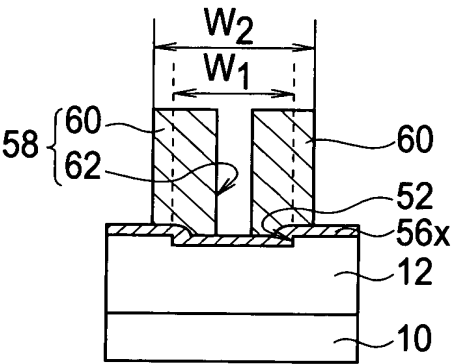


FIG. 6(D)

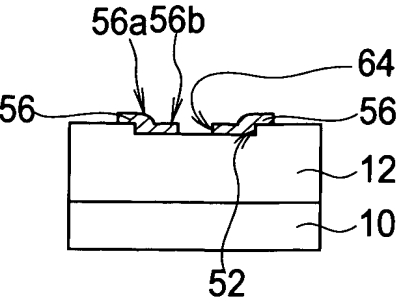


FIG. 7(A)

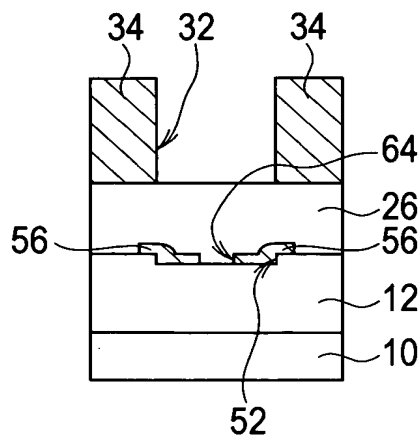


FIG. 7(B)

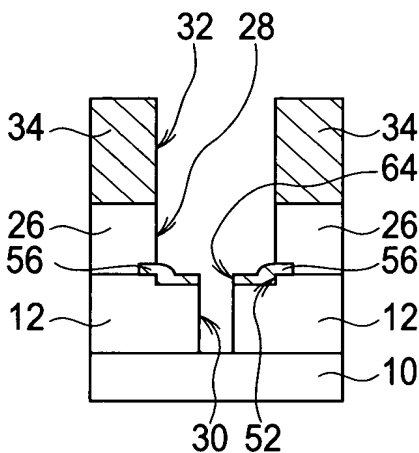


FIG. 7(C)

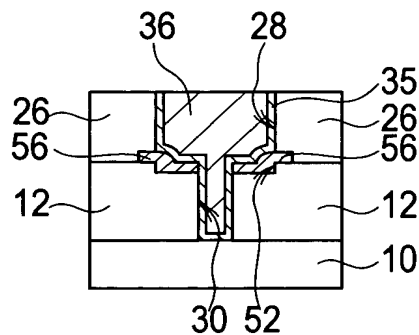


FIG. 8(A)

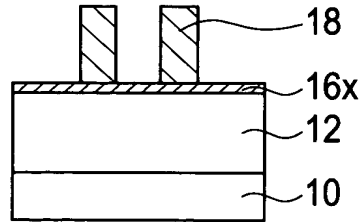


FIG. 8(B)

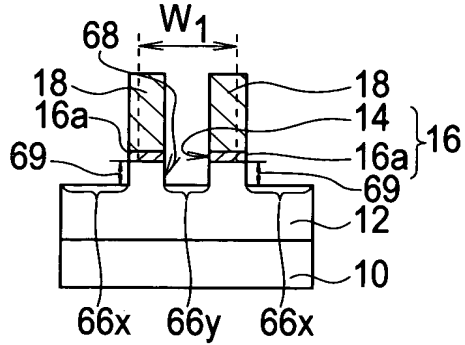


FIG. 8(C)

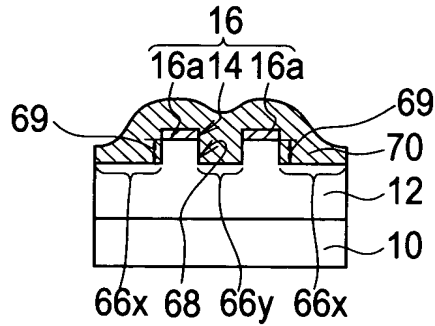


FIG. 8(D)

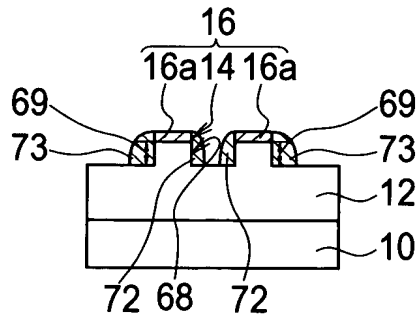


FIG. 9(A)

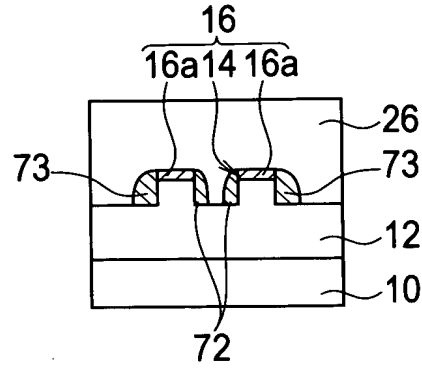


FIG. 9(B)

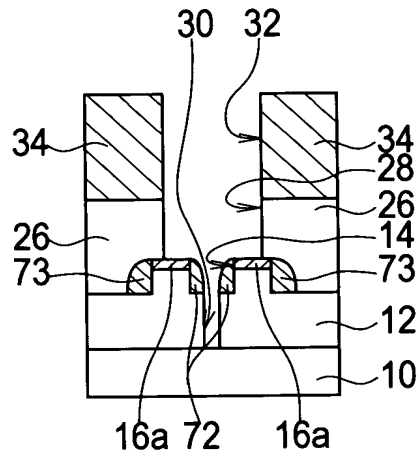
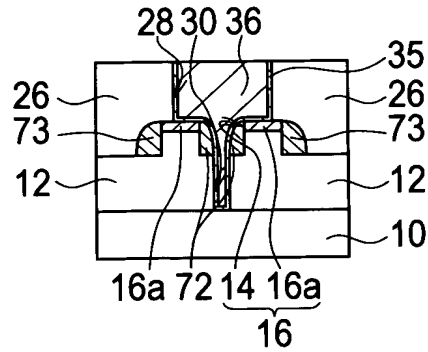


FIG. 9(C)



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FIG. 10(A)

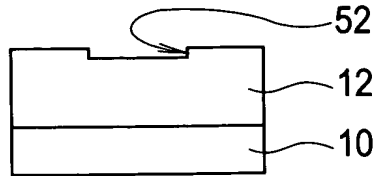


FIG. 10(B)

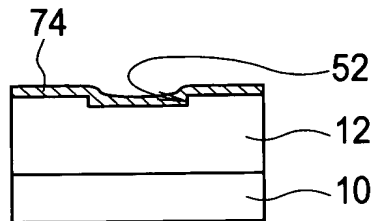


FIG. 10(C)

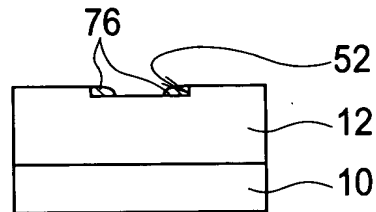
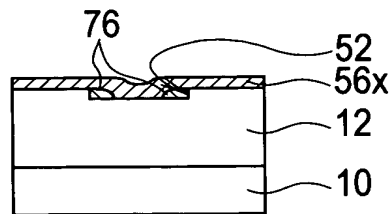


FIG. 10(D)



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FIG. 11(A)

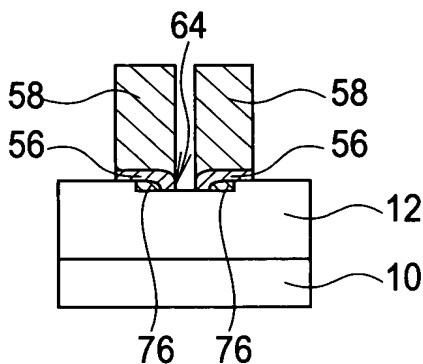


FIG. 11(B)

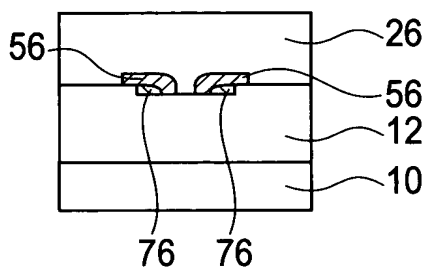


FIG. 11(C)

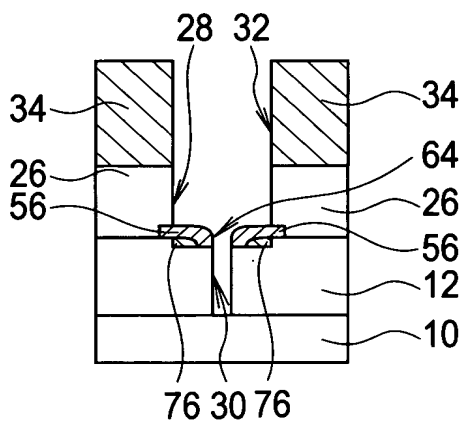
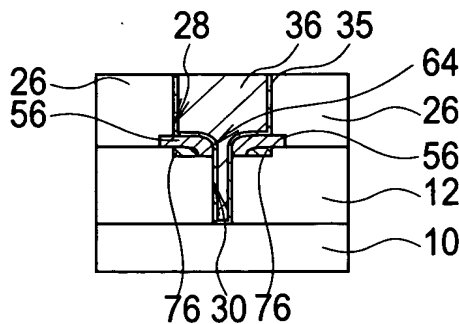


FIG. 11(D)



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FIG. 12(A)

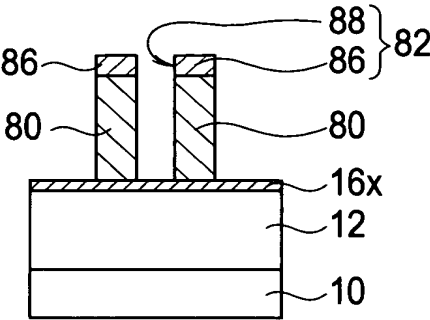


FIG. 12(B)

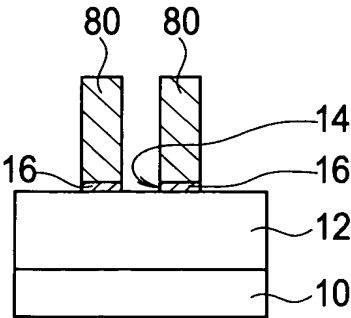


FIG. 12(C)

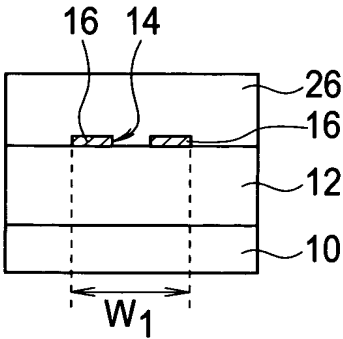


FIG. 13(A)

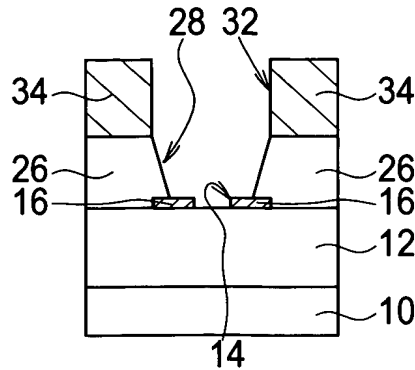


FIG. 13(B)

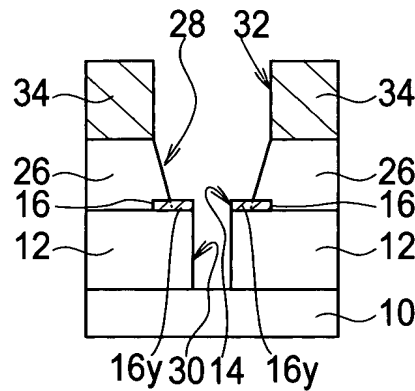


FIG. 13(C)

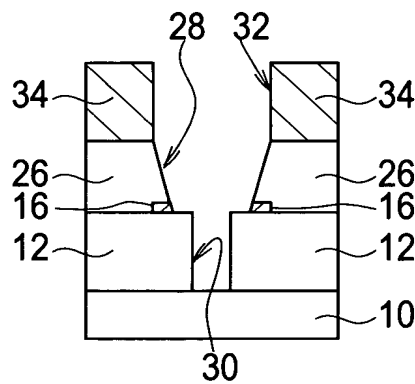


FIG. 13(D)

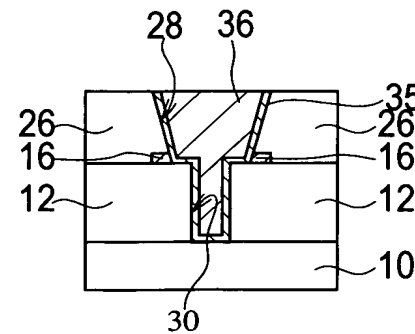
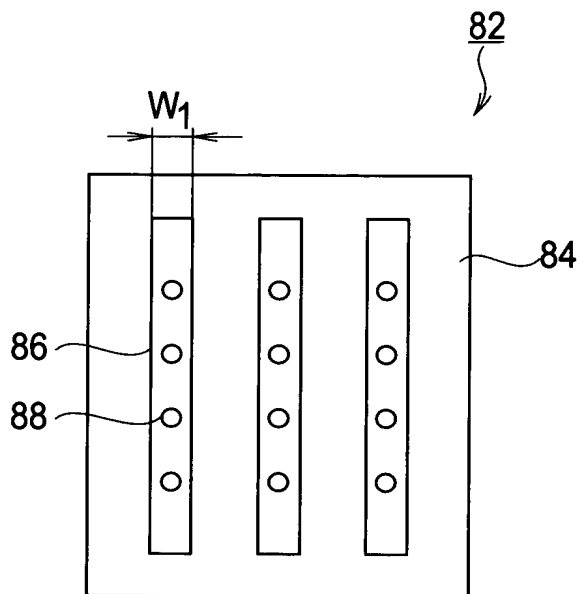


FIG. 13(A) is a cross-sectional view of a semiconductor device in a first embodiment. FIG. 13(B) is a cross-sectional view of a semiconductor device in a second embodiment. FIG. 13(C) is a cross-sectional view of a semiconductor device in a third embodiment. FIG. 13(D) is a cross-sectional view of a semiconductor device in a fourth embodiment.

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FIG. 14



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 Semiconductor Device and Semiconductor Device Manufacturing Method
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FIG. 15(A)

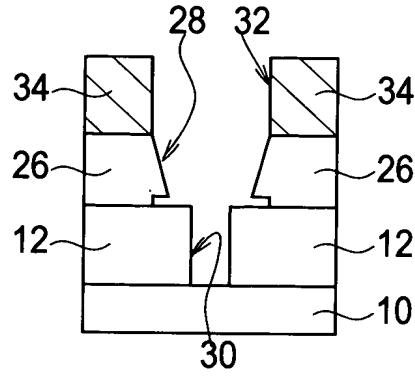
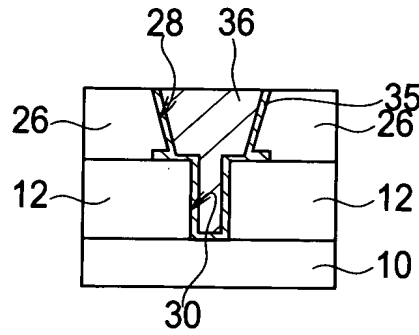


FIG. 15(B)



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FIG. 16(A)

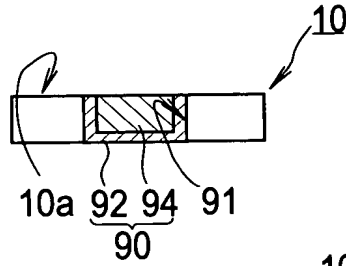


FIG. 16(B)

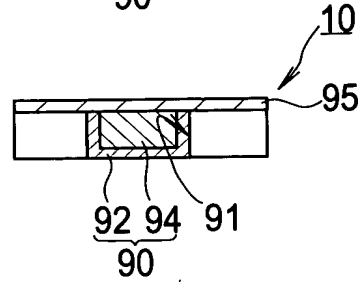


FIG. 16(C)

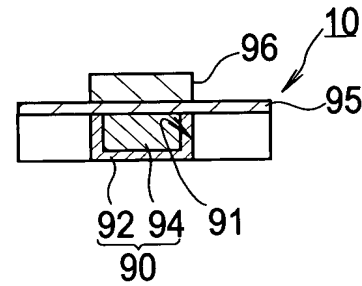


FIG. 16(D)

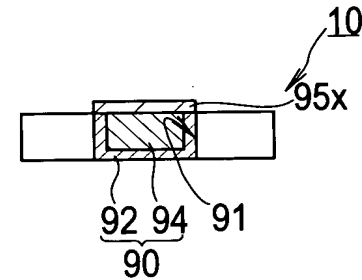


FIG. 16(A) is a cross-sectional view of a semiconductor device structure 10. The structure 10 includes a substrate 10a and a central region 90. The central region 90 includes layers 92 and 94, and is flanked by regions 91. A curved arrow indicates a process step.

FIG. 17(A)

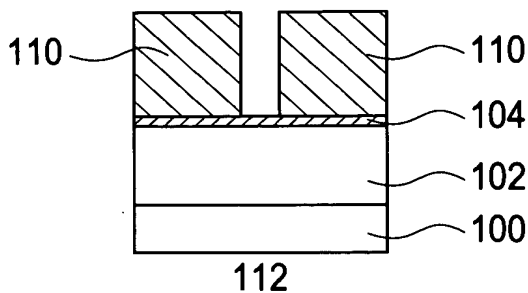


FIG. 17(B)

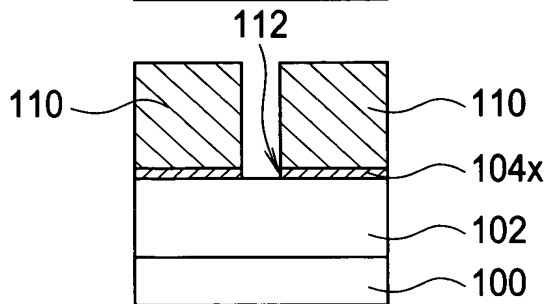


FIG. 17(C)

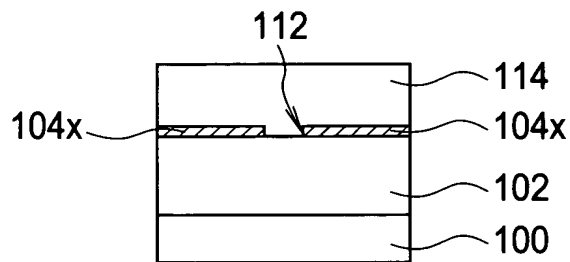


FIG. 17(D)

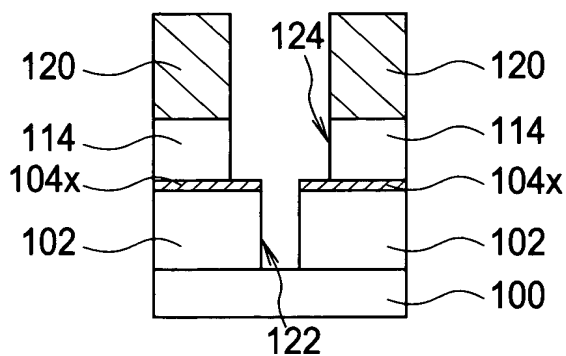


FIG. 17(E)

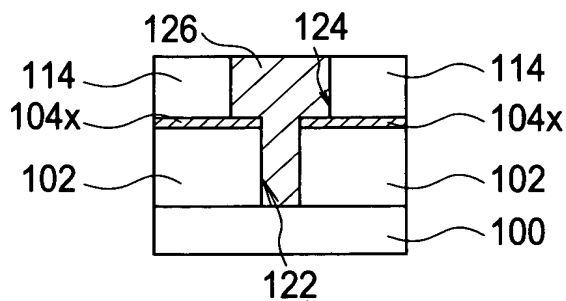


FIG. 18

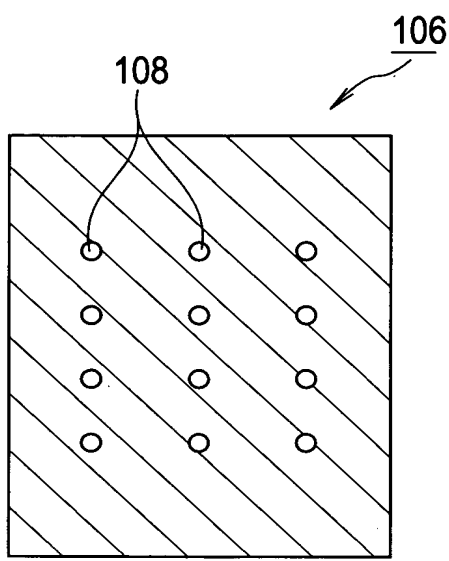
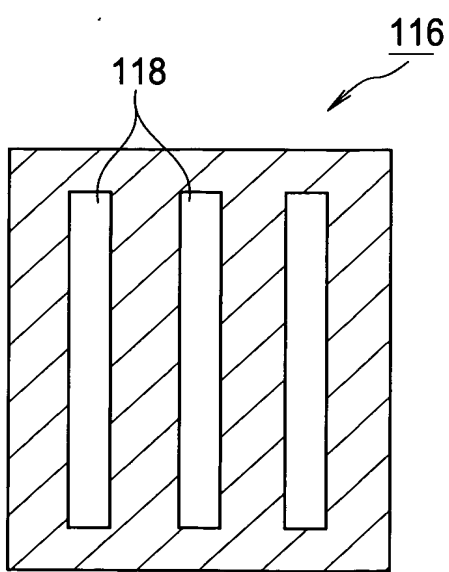


FIG. 19



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FIG.20

